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Passivation of InGaAs(001)-(2 × 4) by Self-Limiting Chemical Vapor Deposition of a Silicon Hydride Control Layer

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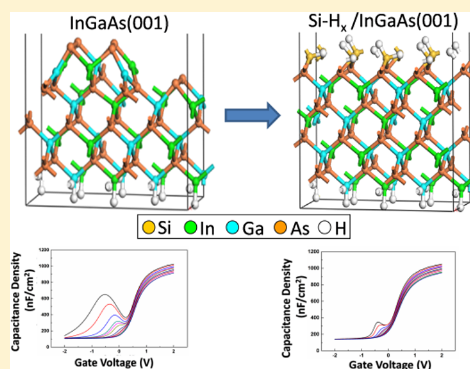
Supporting Information

ABSTRACT: A saturated Si−H_x seed layer for gate oxide or contact conductor ALD has been deposited via two separate self-limiting and saturating CVD processes on InGaAs(001)-(2 × 4) at substrate temperatures of 250 and 350 °C. For the first self-limiting process, a single silicon precursor, Si_3H_8, was dosed at a substrate temperature of 250 °C, and XPS results show the deposited silicon hydride layer saturated at about 4 monolayers of silicon coverage with hydrogen termination. STS results show the surface Fermi level remains unpinned following the deposition of the saturated silicon hydride layer, indicating the InGaAs surface dangling bonds are electrically passivated by Si−H_x. For the second self-limiting process, Si_2Cl_6 was dosed at a substrate temperature of 350 °C, and XPS results show the deposited silicon chloride layer saturated at about 2.5 monolayers of silicon coverage with chlorine termination. Atomic hydrogen produced by a thermal gas cracker was subsequently dosed at 350 °C to remove the Si−Cl termination by replacing with Si−H termination as confirmed by XPS, and STS results confirm the saturated Si−H_x bilayer leaves the InGaAs(001)-(2 × 4) surface Fermi level unpinned. Density function theory modeling of silicon hydride surface passivation shows an Si−H_x monolayer can remove all the dangling bonds and leave a charge balanced surface on InGaAs.



■ INTRODUCTION

InGaAs intrinsically has very high electron mobility, making it a leading material for replacement of silicon as the n-type channel of metal oxide semiconductor field effect transistors (MOSFETs).[1−3] Subnanometer FET devices have lower threshold voltages thereby making trap and fixed charge elimination critical.[4−7] The III−V(001) surfaces are dominated by relatively unreactive filled and empty dangling bonds while the group IV dangling bonds are half-filled and, therefore, highly reactive. The high reactivity of the group IV dangling bonds facilitates their elimination during deposition of gates oxides. Therefore, it is proposed that a thin layer (2−4 monolayers) of epitaxial crystalline silicon on InGaAs or related materials (GaAs or InAs) could facilitate dangling bond elimination and formation of a passive interface.

Previous work has shown the deposition of a thin molecular beam epitaxy (MBE) silicon interfacial control layer on the clean $In_{0.53}Ga_{0.47}As(100)$ surface prior to SiO_2 deposition serves to reduce surface Fermi level pinning.[7,8] Deposition of a thin MBE silicon layer on $In_{0.53}Ga_{0.47}As(100)$ prior to Al_2O_3 deposition leads to improved MOSFET device performance by decreasing frequency dispersion, reducing hysteresis, and lowering D_{it}.[8] Similarly, previous reports also show the physical vapor deposition (PVD) of an a-silicon passivation layer prior to deposition of a bilayer gate insulator stack (1 nm Al_2O_3/5 nm HfO_2) passivates $In_{0.53}Ga_{0.47}As$, as C−V characteristics showed inversion and low D_{it}, and XPS results show no III−V oxide formation.[9] Ex situ deposition of a thin ∼1.2 nm a-silicon layer by PECVD on $In_{0.53}Ga_{0.47}As$ prior to Al_2O_3 gate oxide ALD has been shown to suppress gallium suboxide formation, and MOSFET devices exhibit higher drive current and higher effective electron mobility values.[10,11] Detailed XPS studies have shown the presence of Ga_2O_3 at the interface of both GaAs and $In_{0.53}Ga_{0.47}As$ based MOSFET devices leads to high frequency dispersion and consequently high D_{it}, while an ex situ deposition (PECVD) of an a-silicon layer on GaAs/$In_{0.53}Ga_{0.47}As$ surfaces eliminates Ga +3 oxide formation and significantly lowers frequency dispersion while increasing device drive current in MOSFET C−V measurements.[12]

Si based interface control layers have also been investigated on GaAs(100) based MOSFET devices by PVD and PECVD techniques. PVD of multilayer silicon has been used to passivate GaAs(100), but this method has been shown to

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require a minimum thickness of 1.5 nm in order to effectively passivate the III−V surface and protect against oxygen diffusion to the III−V surface and the concomitant formation of high D_{it} during high temperature annealing.[13,14] GaAs(100) based MOSFET devices with a 1.2 nm a-silicon passivation layer deposited by ex situ plasma enhanced chemical vapor deposition (PECVD) prior to Al_2O_3 gate oxide ALD have been fabricated and show low frequency dispersion, negligible false inversion, and high drive current as the silicon layer gets oxygen, protecting from higher III−V oxidation states.[15,16]

The silicon MBE and PVD processes leave the surface terminated with unpassivated silicon atoms which have half-filled dangling bonds which pin the Fermi level and readily react with trace gases such as H_2O. Chemical vapor deposition (CVD) processes expose the substrate to one or more gaseous precursors in order to grow conformal thin films at a given temperature. CVD growth is usually not limited to a single atomic layer, as heterogeneous and homogeneous surface reactions may occur. In an atomic layer deposition (ALD) process, precursors and growth temperature are chosen to inhibit gas phase reactions and to limit chemical reactivity to heterogeneous surface species. An ALD reaction always employs two precursors, one an oxidant and one a reductant, which are dosed in separate "half-reactions" to avoid homogeneous reactions. Surface dangling bonds are terminated at each ALD half-cycle reaction; since one reactant is an oxidant while the other is a reductant, each heterogeneous half-cycle is self-limiting. At the end of the ALD process, the surface is terminated with one of the ALD precursors and usually no dangling bonds. Consequently, ALD allows deposition of silicon with dangling bonds already passivated by ALD precursor ligands thereby providing chemical passivation.

Commercial ALD flow-type reactors operate at 0.75−7.5 torr where one ALD cycle consists of a pulse of the first ALD precursor, followed by an inert gas purge to remove traces of unreacted precursor and gaseous byproducts, followed by a pulse of the second ALD precursor and a subsequent inert gas purge.[17] Many *Surf. Sci.* reports include self-limiting and saturating atomic layer deposition half-cycle reactions in a high vacuum (base pressure $<10^{-3}$ torr) or ultrahigh vacuum environment (base pressure $< \sim 10^{-9}$ torr) and will be referred to here as HV-ALD or UHV-ALD. The high/ultrahigh vacuum environment aides in protecting the substrate and deposited thin films from unwanted contaminants which may be more prevalent in higher base pressure systems. In HV-ALD or UHV-ALD, the inert gas purge steps are usually replaced by simple vacuum purge steps. Previously, a silicon HV-ALD growth process was reported on SiO_2 using alternate pulses of Si_2H_6 and $SiCl_4$ at substrate temperatures of 355−385 °C, and each ALD cycle required several minutes as formation of the HCl(g) byproduct is slow below 400 °C.[18] Silicon UHV-ALD was reported on Ge substrates by alternating pulses of Si_2Cl_6 and atomic hydrogen or by alternating pulses of SiH_2Cl_2 and SiH_4 at substrate temperatures of 400−560 °C.[19,20] Silicon UHV-ALD processes on Si substrates have been reported with alternating pulses of SiH_2Cl_2 and atomic hydrogen or by alternating pulses Si_2H_6 and Si_2Cl_6, at substrate temperatures (400−560 °C).[21,22] These HV/UHV-ALD processes employ high substrate temperatures which probably desorb the passivating ligand and may cause changes in substrate reconstruction or composition for InGaAs and related materials.[23]

In this report, a self-limiting and saturating HV-CVD process using a single silicon ALD precursor (Si_3H_8) at a low substrate temperature of 250 °C is compared with a second self-limiting and saturating HV-CVD growth process employing the silicon precursor, Si_2Cl_6, at a substrate temperature of 350 °C. The Si_3H_8 process results in depositing a saturated thin silicon hydride capping layer (approximately 4 monolayers) on the InGaAs(001)-(2 × 4) surface and leaving the surface Fermi level unpinned and ready for subsequent atomic layer ALD of the gate oxide. Once the Si−H groups passivate substrate dangling bonds, saturation occurs because H_2 desorption from silicon dihydride is slow at 250 °C and H_2 desorption from silicon monohydride species does not occur below 445 °C.[24] The Si_2Cl_6 self-limiting CVD process results in a thin saturated silicon bilayer deposited on the InGaAs(001)-(2 × 4) surface, and the InGaAs surface is left terminated with Si−Cl groups. Atomic hydrogen produced by a thermal gas cracker is subsequently dosed at 350 °C to quickly remove the Si−Cl termination by replacing with Si−H termination through a ligand exchange reaction resulting in the HCl(g) desorption byproduct. This process also leaves the surface Fermi level unpinned and ready for subsequent surface functionalization with an oxidant or further silicon multilayer growth by ALD. As far as we know, this is the first report of epitaxial deposition of 2−4 layers of silicon with hydrogen termination by self-limiting CVD; the process is inherently self-limiting because it takes advantage of the low desorption temperature of hydrogen and chlorine from InGaAs relative to silicon.

■ EXPERIMENTAL DETAILS

This study employs n-type (Si dopant) and p-type (Be dopant) samples consisting of 0.2 μm of $1-2 \times 10^{18}$ doped $In_{0.53}Ga_{0.47}As$ layers grown by MBE on commercially available InP substrates. The samples were capped with a 50 nm As^2 layer and shipped/stored under vacuum prior to being loaded into the Omicron ultrahigh vacuum (UHV) preparation chamber with a base pressure of 1×10^{-10} torr. In the preparation chamber, the samples were degassed at 250 °C for 30 min and, subsequently, decapped and annealed for 1 h by radiatively heating at 360−370 °C to obtain the InGaAs(001)-(2 × 4) surface reconstruction.

Following annealing, the samples were characterized by an Omicron in situ monochromatic XPS using the aluminum Kα excitation source ($h\nu$ = 1486.7 eV) with spectra taken at a glancing angle of 30° to obtain enhanced surface sensitivity. XPS raw counts were collected using the XPS constant analyzer energy mode with a pass energy of 50 eV and line width of 0.1 eV. XPS peak shape analysis was conducted using CASA XPS v.2.3 by employing a Shirley background subtraction. All XPS raw core level peaks were corrected by Schofield photoionization cross-sectional relative sensitivity factors. Oxygen contamination was monitored over the course of the experiments by XPS, and percentages were calculated by dividing the O 1s corrected peak area by the sum of the As 2p, Ga 2p, In 3d, and Si 2p corrected peak areas. For the Si_3H_8 process, the percent O was below the XPS detection limit, and for the Si_2Cl_6 process, the percent O was <5% (see Supporting Information). Carbon contamination for both processes was below the XPS detection limit. Following XPS elemental analysis of the surface, the samples were transferred to the SPM analysis chamber which has a base pressure of 2×10^{-11} torr. In the SPM chamber, scanning tunneling microscopy (STM) was performed at 300 K to determine the atomic order of the surface by using constant current mode with the tunneling current set point at 0.1 nA, and the sample bias set to −3 V for filled state imaging. Scanning tunneling spectroscopy (STS) was performed to determine the electrical quality of the surface and probe the local surface density of states using variable-*z* mode with the sample bias swept from −1.5 to +1.5 V and the tip simultaneously moving toward and then away from the

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surface.[25] An applied Δz initial offset ranging from −0.2 to −0.8 nm was used in order to maximize $I(V)$ signal without crashing the STM tip. The dI/dV spectra were recorded using a lock-in amplifier, and STS curves are reported by averaging 10−12 single curves taken across the sample surface.

After initial characterization, the samples were transferred back to the preparation chamber and radiatively heated to 250 or 350 °C for 15 min while simultaneously the high vacuum ALD chamber manipulator was also heated to 250 or 350 °C for 15 min to facilitate a faster sample transfer. Prior to sample transfer to the HV-ALD chamber, Si_3H_8 or Si_2Cl_6 were prepulsed in the ALD dosing chamber to coat the chamber walls with precursor prior to sample transfer. This preheating and prepulsing procedure was done before every dose of Si_3H_8 or Si_2Cl_6.

Both processes are referred to as CVD processes because the InGaAs substrate undergoes some surface induced etching by hydrogen or chlorine dissociated ligands from Si_3H_8 or Si_2Cl_6, keeping these processes from classification as true ALD.[26,27] The HV-CVD processes include the substrate in the HV-ALD chamber (base pressure $<2 \times 10^{-7}$ torr) undergoing exposure to Si_3H_8 or Si_2Cl_6 at 250 or 350 °C with the exposure measured in langmuirs (1×10^{-6} torr/1 s, or L) by a convectron gauge located adjacent to the HV-ALD chamber. The HV-CVD process transfers well into a commercial ALD tool as demonstrated in the Beneq TFS-200 continuous flow reactor where MOSCAP fabrication employing the Si_2Cl_6 based passivation process was demonstrated (see Supporting Information). For the saturating Si_3H_8 based process, the sample was transferred into the HV-ALD dosing chamber, and 13 megalangmuir (ML) Si_3H_8 was dosed at 250 °C. Following Si_3H_8 dosing, the sample was transferred back to the preparation chamber where XPS was performed. Following an initial 13 ML Si_3H_8 dose, the sample was exposed to a series of additional doses at 250 °C to increase the integrated dose to 50, 100, and 300 ML of Si_3H_8. The 13, 50, and 100 ML total Si_3H_8 doses consisted of 10 s pulses of 7.5×10^{-2} torr, and the 300 ML total dose (additional 200 ML) consisted of 10 s pulses of 1×10^{-1} torr. After each dose, the sample was transferred to the preparation chamber for XPS studies. After the 300 ML dose, the sample was transferred to the SPM chamber for STM and STS. Following STM and STS of the complete 300 ML dosed surface, the sample was subsequently annealed to 450 °C for 30 min at a heating rate of 2 K/s. During annealing, a mass spectroscopy measurement was taken with a quadropole mass spectrometer equipped with an RGA detector located in the preparation chamber (SRS RGA100). The RGA detector was operated in histogram mode to examine the partial pressure versus mass of detected gas species by sweeping across 0−70 amu. STS was performed to determine any effect on the surface Fermi level position following high temperature annealing. Mass spectroscopy shows 2× higher presence of H_2 species (m = 2 amu) seen during the 30 min 450 °C anneal (see Supporting Information).

For the self-limiting and saturating CVD growth process with Si_2Cl_6, the sample was transferred into the ALD dosing chamber, and 3 ML Si_2Cl_6 was dosed at 350 °C. Following the initial 3 ML Si_2Cl_6 dose, the sample was exposed to a series of additional doses at 350 °C to increase the integrated dose to 12 and 21 ML of Si_2Cl_6. After each Si_2Cl_6 dose, the sample was transferred back to the preparation chamber where XPS was performed. The 3, 12, and 21 ML total Si_2Cl_6 doses consist of 10 s pulses of 2.5×10^{-2} torr. After the complete 21 ML dose, the sample was dosed with 500 L of atomic hydrogen in order to remove the surface chlorine termination by replacing with hydrogen termination through a ligand exchange reaction creating an HCl(g) byproduct. An Oxford Applied Research TC-50 thermal gas cracker was employed to produce atomic hydrogen and was operated at 65 W, producing atomic hydrogen at 50% efficiency. The 500 L dose consists of $H_2(g)$ flowed for 8 min and 20 s at an H_2 pressure of 1×10^{-6} torr; note the calculated langmuirs does not include the H cracking fraction since this could not be experimentally verified so the reported atomic H langmuirs are an upper limit.

The density-functional theory (DFT) simulations were performed using VASP plane-wave DFT simulation package with projector augmented-wave (PAW) pseudopotentials[28−33] and PBE exchange-correlation functional.[34] The InGaAs was a regular polymorph with 50% Ga and 50% In. Initially, the InGaAs unitcell was optimized at variable volume to avoid internal compression/strain. The optimized unitcell was later used to build the InGaAs supercell and initial slabs with desired surfaces. All slab relaxations were performed using conjugate-gradient relaxation algorithm with a force tolerance level of 0.05 eV/Å and gamma-centered 5 × 7 × 1 K-point grid. During relaxations the three bottom layers of InGaAs slabs were permanently fixed in their bulklike positions and saturated with pseudo-H atoms with 1.25 |e| charge to simulate continuous bulk. The Si atoms at upper surfaces were passivated by normal 1.0 |e| H atoms. To avoid possible dipoles, dipole correction in vertical Z direction was applied.

RESULTS

Figure 1a shows the raw XPS peak areas for Ga 3p and Si 2p peaks on the clean (2 × 4) surface, and following 13, 50, 100, and 300 ML Si_3H_8 doses. The Ga 3p spin orbit split peaks are located at binding energies 104.4 and 107.9 eV, and the Si 2p peak is located at a binding energy of 99.5 eV. With each additional dose, the Si 2p peak area increases and the substrate Ga 3p peak decreases, indicative of increasingly higher surface coverage of SiH_x groups. Figure 1b shows the corrected XPS peak areas for the clean n-type InGaAs(001)-(2 × 4) surface, and following 13, 50, 100, and 300 ML Si_3H_8 doses. In 3d, Ga 2p, and As 2p higher binding energy peaks were chosen in order to analyze the topmost monolayers of the surface. The corrected peak area of In 3d is about three times higher than Ga 2p and As 2p corrected peak areas on the clean decapped surface consistent with the In 3d having a binding energy less than half the binding energy of Ga 2p and As 2p (therefore a greater probe depth), as well as the reported phenomenon that indium segregates to the topmost surface layers of InGaAs(001) alloys.[35−37] The decrease in the In 3d, Ga 2p,

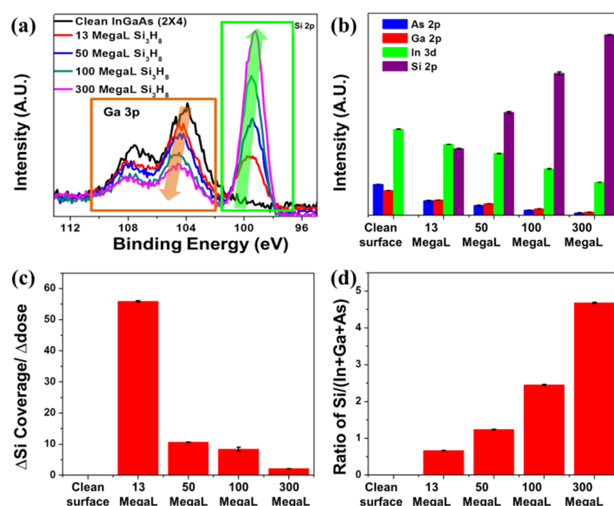

Figure 1. XPS of Si_3H_8 dosed InGaAs(001)-(2 × 4). XPS raw counts are corrected by Schofield photoionization cross-sectional relative sensitivity factors. (a) Raw XPS peak areas for Ga 3p and Si 2p on clean InGaAs(2 × 4), and following 13, 50, 100, and 300 ML total Si_3H_8 doses at 250 °C. (b) XPS corrected peak areas for 13, 50, 100, and 300 ML total Si_3H_8 doses at 250 °C on n-type InGaAs(001)-(2 × 4). (c) Rate of change of silicon coverage versus total Si_3H_8 dose as calculated from XPS corrected Si 2p peak areas for 13, 50, 100, and 300 ML total Si_3H_8 doses at 250 °C on n-type InGaAs(001)-(2 × 4). (d) XPS corrected peak area ratio of Si/(In+Ga+As) for clean (2 × 4), 13 ML Si_3H_8, 50 ML Si_3H_8, 100 ML Si_3H_8, and 300 ML Si_3H_8 total doses at 250 °C. Note error bars are standard errors.

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and As 2p substrate peaks with an increase in silicon coverage is consistent with a uniform surface coverage of silicon. The Si 2p corrected peak area following the 13 ML Si_3H_8 dose is half that of the total In, Ga, and As combined substrate peak areas. The total 300 ML Si_3H_8 dose is 23 times the initial 13 ML dose, yet the increase in silicon coverage is only 2.7. The XPS data is consistent with a self-limiting CVD growth process.

To further quantify the saturation, Figure 1 c shows change in silicon coverage versus Si_3H_8 dose for 13, 50, 100, and 300 ML total doses on n-type InGaAs(001)-(2 × 4) at 250 °C. The change in silicon coverage was calculated for each Si_3H_8 dose by dividing the increase in corrected Si 2p peak area by the increase in dose.

The thickness of the deposited silicon capping layer can be calculated from the equation $\ln(I/I_o) = -t/\lambda$, where I is the sum of the intensity of the In 3d, Ga 2p, and As 2p peaks following each Si_3H_8 dose, I_o is the sum of the intensity of the In 3d, Ga 2p, and As 2p peaks on the clean InGaAs(001)-(2 × 4) surface, t is the thickness of the deposited silicon layer, and λ is the inelastic mean free path of the collected electrons of the InGaAs substrate (1 nm). Using this equation, the total 300 ML Si_3H_8 dose saturates at about 4.5 monolayers of silicon coverage with hydrogen termination. The calculated silicon thickness closely corresponds with the ratios shown in Figure 1d.

Figure 2a shows a filled state STM image of the clean InGaAs(001)-(2 × 4) surface, and Figure 2b shows 300 ML Si_3H_8 dosed on the p-type InGaAs(001)-(2 × 4) surface at 250 °C with no further annealing. Vertical ordering along the same direction as the underlying substrate arsenic dimer (2 × 4) rows is observed in regions across the STM image. Five line traces are taken across these ordered regions (Figure 2c). Spacing between ordered rows is nearly identical to the clean (2 × 4) surface with average spacing at 1.5 ± 0.26 nm consistent with III−V dangling bond elimination through silicon bonding in a commensurate structure with the substrate in regions across the surface. Line traces were measured across the surface as shown in Figure 2d; surface features vary in height by one atomic step (~2.3 ± 0.2 Å standard error) showing high surface uniformity. Previous STM studies of MBE silicon growth on the GaAs(001)-(2 × 4) surface show silicon absorbs in localized heteroepitaxial ordered structures across the (2 × 4) surface with several surface reconstructions present, consistent with our finding of local surface epitaxy.[38] As shown in previous work, epitaxial growth of silicon on the $In_{0.53}Ga_{0.47}As$ surface is not required for surface passivation and improving MOSFET device performance.[7−11] This self-limiting CVD process using Si_3H_8 results in local surface epitaxy as shown with both STM and XPS measurements, as the Si 2p peak shows resolved spin−orbit splitting (see Supporting Information).[39]

Figure 2 e shows the STS measurements probing the local surface density of states of the n-type decapped InGaAs(001)-(2 × 4) surface before and after a saturated 300 ML Si_3H_8 dose at 250 °C. It has previously been shown that InGaAs(001)-(2 × 4) based MOSFETs exhibit good Fermi level modulation characteristics, indicating the InGaAs(001)-(2 × 4) surface Fermi level is unpinned.[40] The conduction and valence band edges align with that of the clean surface showing a saturation Si_3H_8 dose at 250 °C leaves the surface Fermi level unpinned. Figure 2e also shows subsequently annealing the saturated 300 ML Si_3H_8 on n-type InGaAs(001)-(2 × 4) surface to 450 °C for 30 min causes the surface Fermi level to shift toward midgap, indicative of surface dangling bonds created by desorption of $H_2(g)$ from silicon due to the high temperature annealing. Similar results are seen on the p-type InGaAs(001)-(2 × 4) surface showing the surface Fermi level also remains unpinned and p-type following a saturation 300 ML Si_3H_8 dose at 250 °C (Figure 2f). Desorption limited CVD growth occurs at 250 °C, where the presence of any available clean InGaAs surface sites provide a path for H_2 recombinative desorption to occur and further silicon multilayer growth to continue slowly until saturation is found at about 4.5 monolayers of silicon with hydrogen termination. Si−H_3 is the least stable hydride species with desorption on a silicon terminated surface occurring at 225°, leaving Si−H_2 and Si−H groups deposited on the surface which are stable up to 330 °C.[41] H_2 desorption is close to zero at 250 °C on a silicon terminated surface consistent with the surface being saturated with Si−H_2 and Si−H species after all clean InGaAs surface sites have reacted with silicon.[24] The H_2 desorption peak from arsenic-rich surface reconstructions of GaAs(001) starts at 225 °C.[26] The 300 ML total Si_3H_8 dose

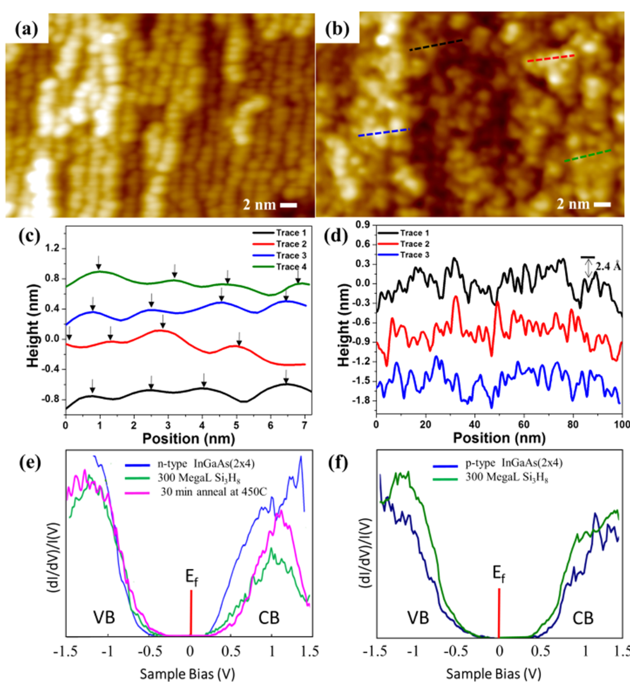

Figure 2. STM/STS of Si_3H_8 dosed InGaAs(001)-(2 × 4). (a) Large area filled state STM image of the clean decapped InGaAs(001)-(2 × 4) surface (b) enlarged area filled state STM images following 300 ML Si_3H_8 dose at 250 °C on p-type InGaAs(001)-(2 × 4) with no further annealing. Dotted lines in (b) indicate rows in which line trace are taken across. Note some ordered rows are shifted 45°, consistent with a mixture of Si−H and Si−H_2 species terminating the surface. (c) Four line traces taken across ordered regions of the surface with average row spacing at 1.5 ± 0.26 nm. Arrows point to the atomic positions in each line trace. (d) Line traces taken across the filled state STM image shown in (b). Surface features vary in height by a maximum of one atomic step (~2.3 ± 0.2 Å). (e) STS results of the decapped n-type InGaAs(001)-(2 × 4) surface, the 300 ML total Si_3H_8 dose at 250 °C, and the 300 MLSi_3H_8 dosed surface following a 30 min anneal at 450 °C (average of 11 STS curves are shown). Note the surface Fermi level shifts toward midgap after annealing, indicative of surface dangling bonds created by increasing the rate of desorption of $H_2(g)$ from silicon. (f) STS results of the decapped p-type InGaAs(001)-(2 × 4) surface before and after the 300 ML total Si_3H_8 dose at 250 °C. The alignment of both the valence and conduction bands and the Fermi level position remains the same on both n-type and p-type surfaces following the saturation dose, indicative of surface passivation.

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(additional 200 ML Si_3H_8 following the total 100 ML Si_3H_8 dose) takes over half an hour to complete at the indicated dosing pressure. This lengthy dose time assists in the slow H_2 desorption from remaining clean InGaAs surface sites and from neighboring Si−H_2 sites, where H_2 recombinatively desorbs at low temperatures until nearly complete surface saturation with Si−H and Si−H_2 species is reached.[24]

Figure 3 a shows the raw XPS peak areas for Ga 3p and Si 2p peaks on the clean (2 × 4) surface, and following 3, 12, and 21 ML Si_2Cl_6 doses. The Ga 3p spin orbit split peaks are located at binding energies 104.4 and 108.2 eV, and the Si 2p spin orbit split peak is located at binding energy 99.8 eV. The Si 2p spin orbit split peaks are well resolved for 12 and 21 ML Si_2Cl_6 total doses, and a new Si 2p chemical state is seen at a higher binding energy (100.5−101 eV) indicative of Si−Cl_x bonding or Si−O_x bonding from the small amount of oxygen contamination seen over the course of the experiment (see Supporting Information).[42,43] With each additional dose, the Si 2p peak area increases and the substrate Ga 3p peak decreases, indicative of increasingly higher surface coverage of silicon until the surface reaches saturation and is left terminated by chlorine. Figure 3b shows the surface composition from XPS for the clean n-type InGaAs(001)-(2 × 4) surface, and following 3, 12, and 21 ML Si_2Cl_6 doses. In 3d, Ga 2p, and As 2p higher binding energy peaks are chosen in order to analyze the topmost monolayers of the surface. Note the decrease in the In 3d, Ga 2p, and As 2p substrate peaks with a concurrent increase in silicon coverage consistent with a uniform surface coverage of silicon. The Si 2p peak area following the 3 ML Si_2Cl_6 dose is about 5/6 that of the total In, Ga, and As combined substrate peak areas. The total 21 ML Si_2Cl_6 dose is 7 times the initial 3 ML dose yet the increase in silicon coverage is only 1.87. The XPS data is consistent with a self-limiting CVD growth process. The XPS data in Figure 3b show that the chlorine signal is negligible following the initial Si_2Cl_6 dose but is more prominent following the 12 and 21 ML doses consistent with excess surface gallium and indium being preferentially etched by chlorine following the initial 3 ML Si_2Cl_6 dose.[27] It is hypothesized that once excess surface gallium and indium have been etched and all clean In, Ga, and As surface sites have reacted with Si−Cl_x groups, the surface becomes saturated by chlorine termination as shown following the total 21 ML Si_2Cl_6 dose. Chlorine desorption from silicon is close to zero at 350 °C.[44]

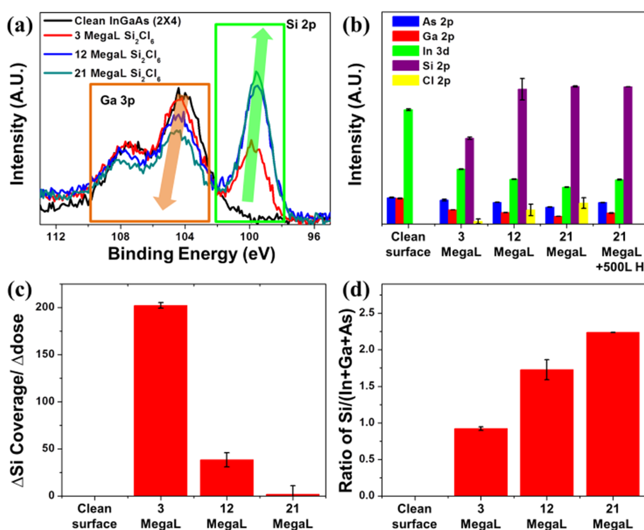

Figure 3. XPS of Si_2Cl_6 dosed InGaAs(001)-(2 × 4). XPS raw counts are corrected by Schofield photoionization cross-sectional relative sensitivity factors. (a) Raw XPS peak areas for Ga 3p and Si 2p on clean InGaAs(2 × 4), and following 3, 12, and 21 ML total Si_2Cl_6 doses at 350 °C. (b) XPS corrected peak areas for 3 ML Si_2Cl_6, 12 ML Si_2Cl_6, 21 ML Si_2Cl_6, and 21 ML Si_2Cl_6 + 500 L atomic hydrogenon n-type InGaAs(001)-(2 × 4). All doses done at 350 °C. (c) Rate of change of silicon coverage versus total Si_2Cl_6 dose as calculated from XPS corrected Si 2p peak areas for 3, 12, and 21 ML total Si_2Cl_6 doses at 350 °C on n-type InGaAs(001)-(2 × 4). (d) XPS corrected peak area ratio of Si/(In+Ga+As) for clean (2 × 4), and 3, 12, and 21 ML total Si_2Cl_6 doses at 350 °C on n-type InGaAs(001)-(2 × 4).

Figure 3c shows change in silicon coverage versus Si_2Cl_6 dose for 3, 12, and 21 ML total doses on n-type InGaAs(001)-(2 × 4) at 350 °C as well as an additional 500 L atomic hydrogen dosed at 350 °C following the total 21 ML Si_2Cl_6 dose at 350 °C. The change in silicon coverage is calculated for each Si_2Cl_6 dose by dividing the increase in corrected Si 2p peak area by the increase in dose. Self-limiting and saturating coverage of silicon on the InGaAs(001)-(2 × 4) surface is seen following the saturated 21 ML Si_2Cl_6 dose as no further increase in the rate of silicon coverage is observed. Similar results are seen on the p-type InGaAs(001)-(2 × 4) surface. Figure 3d shows the Si/(In+Ga+As) XPS peak area ratios for clean n-type (2 × 4), 3, 12, and 21 ML total Si_2Cl_6 doses at 350 °C before and after an additional 500 L atomic hydrogen dose at 350 °C. The ratios shown in Figure 3d correspond with the thickness of the deposited silicon capping layer, which was calculated from the equation $\ln(I/I_o) = -t/\lambda$, where I is the sum of the intensity of the In 3d, Ga 2p, and As 2p peaks following each Si_2Cl_6 dose, I_o is the sum of the intensity of the In 3d, Ga 2p, and As 2p peaks on the clean InGaAs(001)-(2 × 4) surface, t is the thickness of the deposited silicon layer, and λ is the inelastic mean free path of the collected electrons of the InGaAs substrate (1 nm). Using this equation, the total 21 ML Si_2Cl_6 dose saturates at about 2.5 monolayers of silicon coverage.

Figure 4a, b shows filled state STM images of 21 ML Si_2Cl_6 dosed on the n-type InGaAs(001)-(2 × 4) surface at 350 °C followed by 500 L atomic hydrogen dosed at 350 °C with no further annealing. Vertical ordering along the same direction as the underlying substrate arsenic dimer (2 × 4) rows is observed on regions of the surface, and four line traces are taken across these ordered regions (Figure 4c). The spacing between rows is nearly identical to the clean (2 × 4) surface with average spacing at 1.6 ± 0.1 nm consistent with III−V dangling bond elimination through silicon bonding locally in a commensurate structure. Line traces were measured across the surface as shown in Figure 4d; surface features vary in height by one atomic step (∼2.4 ± 0.1 Å), showing high surface uniformity.

Figure 4e shows the STS measurements of the n-type decapped InGaAs(001)-(2 × 4) surface before and after saturation Si_2Cl_6 dosing followed by 500 L atomic hydrogen, and 4 additional 9 ML Si_2Cl_6 + 500 L of atomic H ALD cycles all dosed at 350 °C. The conduction and valence band edges align with that of the clean surface showing a saturation Si_2Cl_6 dose followed by atomic hydrogen dose at 350 °C leaving the surface Fermi level unpinned. Similar results are seen on the p-type InGaAs(001)-(2 × 4) surface showing the surface Fermi level also remains unpinned and p-type following saturation Si_2Cl_6 dosing, 500 L atomic hydrogen, and following an additional 4 Si_2Cl_6 + atomic H ALD cycles all dosed at 350 °C (Figure 4f).

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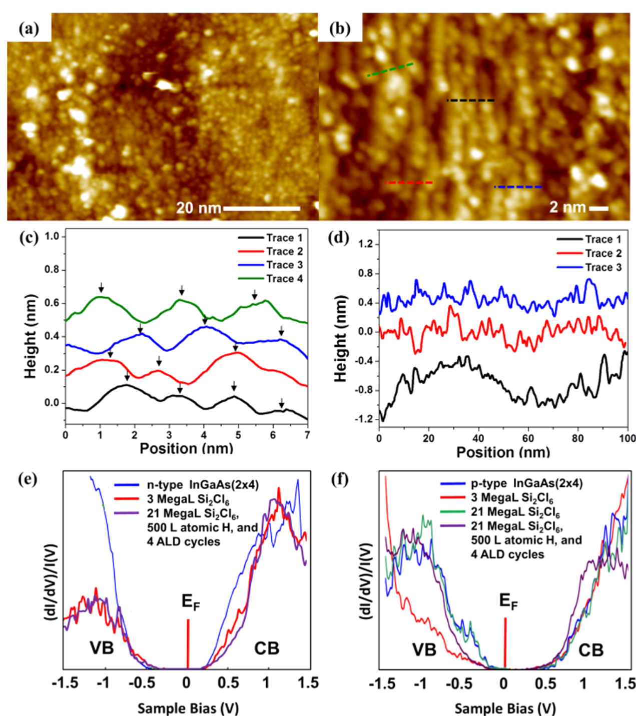

Figure 4. STM/STS of Si_2Cl_6 dosed InGaAs(001)-(2 × 4). (a) Large area and (b) enlarged area filled state STM images following 21 ML Si_2Cl_6 dose at 350 °C and 500 L atomic hydrogen dosed at 350 °C on n-type InGaAs(001)-(2 × 4) with no further annealing. Dotted lines indicate rows in which line traces are taken across. Arrows point to atomic positions in each line trace. Note some ordered rows are shifted 45°, consistent with a mixture of Si−H and Si−H_2 species terminating the surface. (c) Four line traces taken across ordered regions of the surface with average row spacing at 1.6 ± 0.1 nm. (d) Line traces taken across the filled state STM image shown in (a). Surface features vary in height by one atomic step (~2.4 ± 0.1 Å) showing high surface uniformity. (e) STS on n-type InGaAs: clean n-type InGaAs (2 × 4), 3 ML dose of Si_2Cl_6 at 350 °C, 21 ML Si_2Cl_6, 500 L atomic hydrogen, and 4 ALD cycles at 350 °C (an average of 9 STS curves are shown). Each silicon ALD cycle = 9 ML Si_2Cl_6 at 350 °C followed by 500 L atomic H at 350 °C. (f) STS on p-type InGaAs: clean n-type InGaAs (2 × 4), 3 ML dose of Si_2Cl_6 at 350 °C, 21 ML Si_2Cl_6, and 500 L of atomic hydrogen, and an additional 4 ALD cycles at 350 °C (an average of 9−13 STS curves are shown). Note the alignment of both the valence and conduction bands following the saturation dose as well as the Fermi level position remaining the same on both n-type and p-type surfaces indicative of surface passivation.

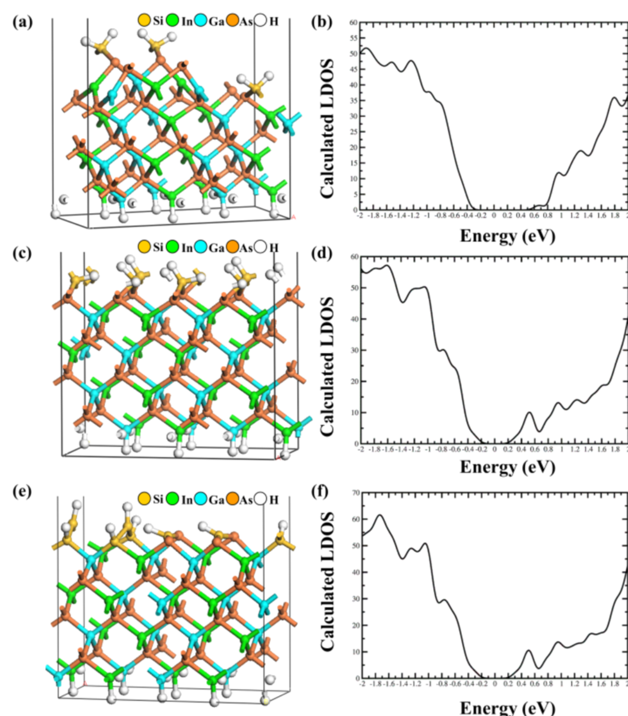

Figure 5. Initial DFT simulations of silicon hydride passivation of InGaAs(001)-(2 × 4). (a) DFT model of partial coverage of Si−H_2 groups passivating the InGaAs(001)-(2 × 4) surface. (b) Calculated local density of states for the partial coverage DFT model shown in (a). Note the Fermi level remains unpinned following partial coverage passivation. (c) DFT model of full coverage of Si−H_2/Si−H groups passivating the InGaAs(001)-(2 × 4) surface. Note the topmost InGaAs surface is arsenic rich with one Si−H group and one Si−H_2 group bonding to each surface arsenic atom. (d) Calculated local density of states for the full coverage DFT model shown in (c). The Fermi level remains unpinned following full coverage passivation. (e) DFT model of full coverage of Si−H_2/Si−H groups passivating the InGaAs(001)-(2 × 4) surface. Note the topmost InGaAs surface contains 1/2 arsenic and 1/2 indium/gallium atoms bonding to Si−H_x groups. (f) Calculated local density of states for the full coverage DFT model shown in (e). The Fermi level remains unpinned following the passivation.

DFT simulations of the initial stages of silicon hydride passivation of the InGaAs(001)-(2 × 4) surface are shown in Figure 5. Figure 5a, b shows partial coverage (less than 1 monolayer) of Si−H_2 groups bonding to surface arsenics. Figure 5c, d shows full monolayer coverage of Si−H and Si−H_2 groups on the InGaAs surface containing As bulklike termination with surface arsenics bonding to a mixture of Si−H and Si−H_2 groups. As seen in XPS results for the Si_2Cl_6 based process, the InGaAs surface is increasingly arsenic rich with each increasing dose of Si_2Cl_6. Following the initial 3 ML Si_2Cl_6 dose, the As 2p peak becomes asymmetric due to the formation of As−Si bonds, leading to a chemical shift of As 2p to a higher binding energy (see Supporting Information). The passivation model shown in Figure 5e, f contains a topmost InGaAs surface layer comprised of 1/2 arsenic and 1/2 indium/gallium atoms bonding to Si−H, consistent with the XPS data from the Si_3H_8 based process showing nearly equivalent amounts of gallium and arsenic on the surface. Following the initial 13 ML Si_3H_8 dose, the As 2p and Ga 2p peaks become asymmetric due to the formation of As−Si and Ga−Si bonds, leading to a chemical shift of As 2p to a higher binding energy and a chemical shift of Ga 2p to a slightly lower binding energy (see Supporting Information). All initial DFT calculations of the silicon hydride passivation of the InGaAs(001)-(2 × 4) surface shown in Figure 5 are in agreement with the STS results showing the surface Fermi level remaining unpinned.

M.D. Pashley described the electron counting model applied to the (In)GaAs(001)-(2 × 4) reconstructed surface which stated surface bonding conditions necessary to maintain no net surface charge, a condition essential to creating an unpinned surface Fermi level.[45] L. Lin and J. Robertson employ this electron counting rule model to create surface interfacial passivating layers on reconstructed semiconductor surfaces by maintaining no net charge for each successive layer of growth.[5] The electron counting rule model has been applied to all DFT models shown in Figure 5 with number of valence electrons for indium/gallium, arsenic, silicon, and hydrogen being 3, 5, 4, and 1. For the partial coverage model shown in Figure 5a, the sp^2

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hybridized indium/gallium surface atoms accommodate the charge deficiency found on each of the sp^3 hybridized arsenic surface atoms. The full monolayer coverage model shown in Figure 5c is comprised of all sp^3 hybridized atoms. Here each surface arsenic bonds to one Si−H group (containing one filled dangling bond) and one $Si{-}H_2$ group, leaving the overall unit cell charge balanced. The full coverage model shown in Figure 5e contains 4 sp^2 hybridized Si−H groups which contain excess electrons to balance the charge deficiency on the sp^3 hybridized surface indium/gallium and arsenic atoms leaving the unit cell charge neutral.

■ CONCLUSION

Deposition of a thin silicon hydride capping layer on InGaAs(001)-(2 × 4) has been achieved via two separate self-limiting CVD processes as shown by XPS. The 250 °C Si_3H_8 process only requires the use of a single ALD precursor, Si_3H_8, with self-limiting growth of 4.5 monolayers of $Si{-}H_x$ coverage achieved at a very low temperature. The Si_2Cl_6 350 °C process produces a thinner $Si{-}H_x$ capping layer (2.5 monolayers) and allows for multilayer silicon growth by ALD through cyclically dosing Si_2Cl_6 and atomic hydrogen. STM and STS measurements show both self-limiting CVD processes on InGaAs(001)-(2 × 4) produce an atomically locally ordered and electrically passivated surface, with the surface Fermi level (E_F) shifting from the valence to the conduction band for p-type vs n-type samples consistent with an unpinned E_F. Initial DFT calculations show the InGaAs(001)-(2 × 4) surface is electronically passivated by $Si{-}H_x$ groups via the satisfaction of the electron counting rule for a charge neutral interface. The calculated local density of states are in agreement with the experimental STS measurements showing the surface Fermi level remains unpinned, and the passivating silicon hydride control capping layer is ready for ALD gate oxide nucleation. Initial MOSCAP fabrication results also show the insertion of a silicon passivation layer by dosing Si_2Cl_6 on the InGaAs(001) surface prior to the deposition of Al_2O_3 leads to lower frequency dispersion, higher C_{max}, and a smaller false inversion indicative of lower D_{it} at midgap.[46] The initial device results show the deposited silicon layer with hydrogen termination seeds high-K gate oxide nucleation and improves device performance.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Figures S1−S6 as described in the text. The Supporting Information is available free of charge on the ACS Publications website at DOI: 10.1021/jacs.5b03660.

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Notes

The authors declare no competing financial interest.

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